AMENDMENT TRANSMITTAL LETTER

Docket No. M4065.0067/P067			
Application No. 09/118,080	Filing Date July 17, 1998	Examiner A. Chambliss	Group Art Unit 2814

Applicant(s): Warren M. Farnworth

OIPE JC100 JAN 12 2001 PATENT & TRADEMARK OFFICE

Invention: LEAD OVER CHIP SEMICONDUCTOR DEVICES WITH A BALL GRID ARRAY (As Amended)

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	32	- 33 =		x	
Independent Claims	6	- 6 =		x	
Multiple Dependent Claims (check if applicable) ☐					
Other fee (please specify):					
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					0.00

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☒ Large Entity ☐ Small Entity

☒ No additional fee is required for this amendment.

☐ Please charge Deposit Account No. _____ in the amount of _____.
A duplicate copy of this sheet is enclosed.

☐ A check in the amount of _____ to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 04-1073 as described below. A duplicate copy of this sheet is enclosed.

☒ Credit any overpayment.

☒ Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

Dated: January 12, 2001

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#6/Amdt A 1/30/01 C. McKinney

Docket No.: M4065.0067/P067
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Warren M. Farnworth

Application No.: 09/118,080

Group Art Unit: 2814

Filed: July 17, 1998

Examiner: A. Chambliss

For: LEAD OVER CHIP SEMICONDUCTOR DEVICES WITH A BALL GRID ARRAY (As Amended)

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AMENDMENT

BOX NON-FEE AMENDMENT
Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

In response to the Office Action dated October 12, 2000 (Paper No. 5), please amend the above-identified U.S. Patent application as follows:

IN THE TITLE

Delete the existing title and rewrite it as: --LEAD OVER CHIP SEMICONDUCTOR DEVICES WITH A BALL GRID ARRAY--.

IN THE SPECIFICATION

For line numbers, please count lines of text as they appear on the page since the margin line numbering appears to be inaccurate.

At page 7, line 15, delete "24-30" and insert --24, 26, 28, 30--.

At page 7, line 16, delete "24-30" and insert --24, 26, 28, 30--.

At page 8, line 19, delete "24-30" and insert --24, 26, 28, 30--.

At page 9, line 2, delete "24-30" and insert --24, 26, 28, 30--.

At page 9, line 5, delete "24-30" and insert --24, 26, 28, 30--.

At page 9, line 17, delete "24-30" and insert --24, 26, 28, 30--.

At page 11, line 2, delete "24-30" and insert --24, 26, 28, 30--.

At page 11, line 3, delete "24-30" and insert --24, 26, 28, 30--.

At page 11, line 12, delete "24-30" and insert --24, 26, 28, 30--.

At page 12, line 1, delete "50-56" and insert --50, 52, 54, 56--.

At page 12, line 2, delete "24-30" and insert --24, 26, 28, 30--.

At page 12, line 2, delete "50-56" and insert --50, 52, 54, 56--.

At page 12, line 4, delete "50-56" and insert --50, 52, 54, 56--.

At page 12, line 5, delete "50-56" and insert --50, 52, 54, 56--.

At page 12, line 5, delete "24-30" and insert --24, 26, 28, 30--.

At page 12, line 7, delete "50-56" and insert --50, 52, 54, 56--.

At page 12, line 8, delete "24-30" and insert --24, 26, 28, 30--.

At page 12, line 9, delete "50-56" and insert --50, 52, 54, 56--.

At page 12, line 11, delete "50-56" and insert --50, 52, 54, 56--.

At page 12, line 12, delete "50-56" and insert --50, 52, 54, 56--.

At page 13, line 4, delete "50-56" and insert --50, 52, 54, 56--.

At page 13, line 14, delete "Leads 24-30" and insert --Leads 24, 26, 28, 30--.

At page 13, line 14, delete "leads 24-30" and insert --leads 24, 26, 28, 30--.

At page 13, line 15, delete "50-56" and insert --50, 52, 54, 56--.

At page 13, line 16, delete "24-30" and insert --24, 26, 28, 30--.

IN THE CLAIMS

Please cancel claim 9.

1. (Amended) A semiconductor device, comprising:

a semiconductor chip;

a single dielectric layer;

electrically conductive leads on said dielectric layer; and

a low temperature curing adhesive material between said semiconductor chip and said dielectric layer.

2. (Amended) The semiconductor device of claim 1, wherein said single dielectric layer includes polyimide.

3. (Amended) The semiconductor device of claim 1, wherein said single dielectric layer includes benzocylobutene.

A2

6. (Amended) The semiconductor device of claim 5, further comprising an opening defined in said single dielectric layer, and wherein said bond wires and said resin material are located in said opening.

A3

8. (Amended) A taped semiconductor product, comprising:

integrated circuits formed in semiconductor material;

a tape having openings aligned with said integrated circuits, wherein said tape includes a single dielectric layer and electrically conductive leads, said leads being printed on said single dielectric layer;

bond wires extending through said openings, said bond wires being electrically connected to said integrated circuits; and

adhesive material between said tape and said integrated circuits.

A4 B2

10. (Amended) The taped semiconductor product of claim 8 [9], wherein said adhesive material cures at room temperature.

A5 B3

13. (Amended) A tape for manufacturing semiconductor devices, said

tape comprising:

A5 Concl'd

a single dielectric layer having openings;

electrically conductive leads associated with said openings, said leads being printed on said dielectric layer; and

a low temperature curing adhesive material.

14. (Amended) The tape of claim 13, wherein said single dielectric layer [material] includes polyimide.

15. (Amended) The tape of claim 13, wherein said single dielectric layer [material] includes benzocylobutene.

A6

31. (Amended) A semiconductor device, comprising:

a semiconductor chip;

a single dielectric layer;

electrically conductive leads on said single dielectric layer; and

an anisotropically conductive adhesive material located between said single dielectric layer and said semiconductor chip.

As cancelled

32. (Amended) The semiconductor device of claim 31, further comprising via holes defined in said single dielectric layer, and metal located in said via holes, said metal being connected to said leads.

REMARKS

Claims 1-3, 6, 8, 10, 13-15, and 31-32 have been amended. Claim 9 has been cancelled. Claims 19-30 have been withdrawn from consideration as corresponding to a non-elected group. Thus, claims 1-8, 10-18, and 31-33 remain pending. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications. Claims 1-18 and 31-33 stand rejected as being anticipated by Heo. These rejections are respectfully traversed.

The drawings are objected to as not containing certain reference signs. The specification has been amended so that all reference signs cited in the specification appear in the drawings. Thus, the Examiner is urged to withdraw the objection to the drawings.

The Èxaminer objected to the title of the invention. The title has now been amended to the title suggested by the Examiner. The Examiner is therefore urged to withdraw the objection to the title.

The present invention is directed at the use of a printed tape to form a leads on chip ("LOC") ball grid array ("BGA") semiconductor device. As shown in Figs. 1-2, a semiconductor wafer 10 containing a plurality of semiconductor chips 14 is almost entirely covered by a tape 12. Each chip contains integrated circuits, which are not separately shown on the diagrams. The tape 12 comprises an adhesive layer 20, a single dielectric layer 22, and leads 24, 26, 28, 30. The single dielectric layer 20 provides electrical insulation between the leads 24, 26, 28, 30 and the integrated circuits formed on the

wafer. The single dielectric layer 20 also provides mechanical support and alpha particle protection for the integrated circuits. See page 9, lines 1-6.

Heo is also directed at the formation of leads on chip semiconductor devices. As illustrated in Fig. 2A, Heo utilizes a multi-layer film 20. The multi-layer film 20 is attached to the upper surface of the semiconductor chip 11 by an adhesive. The multi-layer film 20 is comprised of a conductive circuit pattern 26 which is sandwiched between a first non-conductive film 21 and a second non-conductive film 22. See column 4, lines 45-52. Although there are a number of similarities between Heo and the present invention, the printed tape 12 of the present invention is more economical than the multi-layer film 20 of Heo because the printed tape 12 only requires a single dielectric layer 22, in contrast to the first and second non-conductive films 21, 22 of Heo.

Claim 1 as amended recites: "a single dielectric layer." Heo is devoid of any teachings or suggestions regarding the use of a single dielectric layer. Claim 1 should therefore be allowable over the prior art of record. Claims 2-7 depend from claim 1 and are believed to be allowable over the prior art of record for these reasons and because the combination defined in the claims is not shown or suggested by the cited references.

Claim 8 as amended recites: "wherein said tape includes a single dielectric layer and electrically conductive leads, said leads being printed on said single dielectric layer." Heo is devoid of any teachings or suggestions regarding the use of a single dielectric layer. Claim 8 should therefore be allowable over the prior art of record. Claims 10-12 depend from claim 8 and are believed to be allowable over the prior art of record for these reasons

and because the combination defined in the claims is not shown or suggested by the cited references.

Claim 13 as amended recites: "a single dielectric layer having openings." Heo is devoid of any teachings or suggestions regarding the use of a single dielectric layer. Claim 13 should therefore be allowable over the prior art of record. Claims 14-18 depend from claim 13 and are believed to be allowable over the prior art of record for these reasons and because the combination defined in the claims is not shown or suggested by the cited references.

Claim 31 as amended recites: "a single dielectric layer." Heo is devoid of any teachings or suggestions regarding the use of a single dielectric layer. Claim 31 should therefore be allowable over the prior art of record. Claims 32-33 depend from claim 31 and are believed to be allowable over the prior art of record for these reasons and because the combination defined in the claims is not shown or suggested by the cited references.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: January 12, 2001

Respectfully submitted,

By _____

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